TTμL 9022

DUAL J$\overline{K}$ FLIP-FLOP

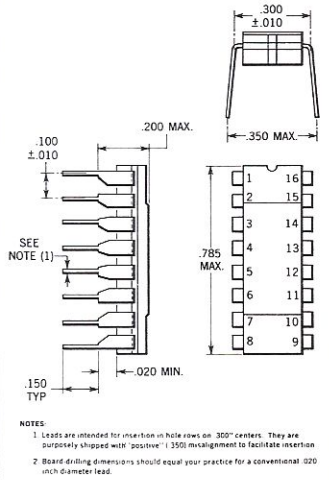
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9022 consists of two J$\overline{K}$ flip-flops with a common clock, separate J and $\overline{K}$ inputs and a common JK input. The J$\overline{K}$ design allows the 9022 to be operated as a D type flip-flop or as a standard J-K flip-flop. Incorporated in the element is a single clock buffer which reduces clock loading.

The joint (JK) input to the flip-flops can be used to advantage for gating information into the flip-flops. It also minimizes clock skew by allowing separate enable control of flip-flops when they are connected to a common clock buss.

PHYSICAL DIMENSIONS

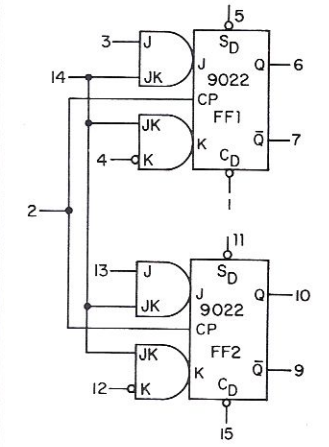


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) mis-alignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES

- 35 MHz operation
- Master-slave circuit
- Common buffered clock input
- Separate J$\overline{K}$ inputs
- Common Input Enable logic
- Separate Direct Clear and Direct set inputs
- The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and MSI families (CCSL).
- All ceramic "HERMETIC" 16-pin Dual In-Line package
- Input Diode Clamping

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +8V
Input Voltage	-0.5V to +5.5V
Voltage Applied to Outputs	-0.5V to V_{CC} Value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION

Specify U6B9022XXX for 16 pin Dual In-Line package where XXX is 51X for the -55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

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TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK 14	J 3(13)	$\overline{K}$ 4(12)	Q 6(10)	$\overline{Q}$ 7(9)
L	X	X	(1)	No Change
H	L	H	(1)	No Change
H	L	L	L	H
H	H	H	H	L
H	H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

H = Most positive logic level

L = Most negative logic level

X = Could be high or low

NOTES:

(1) For no change of outputs, the J and K inputs or the common JK input must remain low ($\overline{K}$ = High) for the entire period in which the clock pulse is at low logic level.

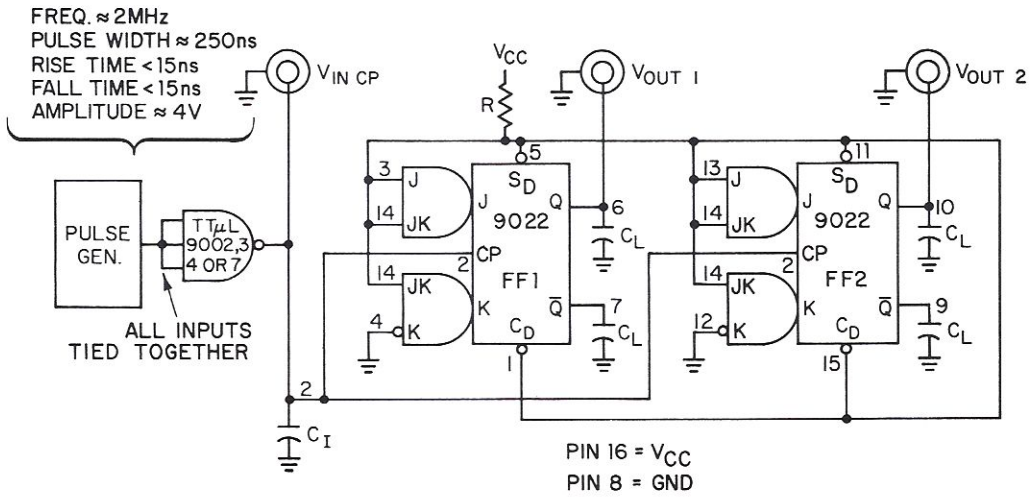
(2) $\overline{K}$ inputs should be grounded when not in use.

LOADING RULES

INPUTS	LOADING
J, $\overline{K}$	1
CP	2
JK	4
C_D & S_D	2.7

OUTPUTS	FANOUT
Q, $\overline{Q}$	10

SWITCHING TIME TEST CIRCUITS



ELECTRICAL CHARACTERISTICS

INDUSTRIAL TEMPERATURE RANGE 0°C to 75°C, V_{CC} 5.0V ±5%

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		0°C		25°C			75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V I_{OH} = -1.2 mA	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs.	
I_R	J,$\overline{K}$ Leakage Current				5	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V	
$2I_R$	Clock Input				10	120		120		Gnd. on other inputs.	
$4I_R$	J-K Input				20	240		240			
I_{RS}	Asynchronous Inputs				14	160		160			
I_F	J,$\overline{K}$ Input Current		-1.60		-1.0	-1.60		-1.60	mA	V_{CC} = 5.25 V	V_F = 0.45 V V_R = 4.5 V on other inputs.
$2I_F$	Clock Input		-3.20		-2.0	-3.20		-3.20			
$4I_F$	J-K Input		-6.40		-4.0	-6.40		-6.40			
I_{FSI}	Asynchronous Inputs		-4.32		-2.7	-4.32		-4.32			
I_F	J,$\overline{K}$ Input Current		-1.41		-0.94	-1.41		-1.41	mA	V_{CC} = 4.75 V	
$2I_F$	Clock Input		-2.82		-1.88	-2.82		-2.82			
$4I_F$	J-K Input		-5.64		-3.76	-5.64		-5.64			
I_{FSI}	Asynchronous Inputs		-3.78		-2.54	-3.78		-3.78			
t_{pd+}					12	22			ns		V_{CC} = 5.0 V C_L = 15 pF
t_{pd-}					21	35			ns		
$t_{release}$					6	1			ns		
t_{set-up}				12	7				ns		
	Negative Clock pulse width			16	11				Toggle Condition		

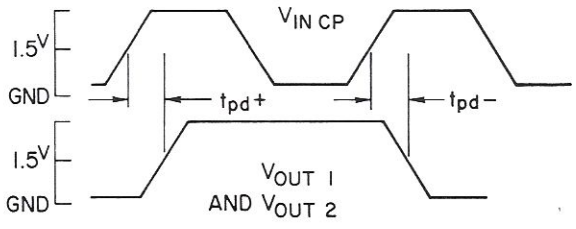
SWITCHING TIME TEST CIRCUITS (Continued)

NOTES:

R = 2K, ±5%, 1/2W
C_I = 15 pF ±5%
C_L = 15 pF ±5%

C_I & C_L include all probe and jig capacity.
Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

WAVEFORMS



ELECTRICAL CHARACTERISTICS

MILITARY TEMPERATURE RANGE −55°C to +125°C, V_{CC} 5.0V ±10%

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
		-55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = -1.2 mA	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.	
I_R	J,$\overline{K}$ Leakage Current				5	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V Gnd. on other inputs.	
$2I_R$	Clock Input				10	120		120			
$4I_R$	J-K Input				20	240		240			
I_{RS}	Asynchronous Inputs				14	160		160			
I_F	J,$\overline{K}$ Input Current		-1.60		-1.1	-1.60		-1.60	mA	V_{CC} = 5.5 V	V_F = 0.4 V
$2I_F$	Clock input		-3.20		-2.2	-3.2		-3.2			
$4I_F$	J-K Input		-6.40		-4.4	-6.40		-6.40			
I_{FSI}	Asynchronous Inputs		-4.32		-3.0	-4.32		-4.32			V_R = 4.5 V
I_F	J,$\overline{K}$ Input Current		-1.24		-0.91	-1.24		-1.24	mA	V_{CC} = 4.5 V	on other inputs
$2I_F$	Clock Input		-2.48		-1.82	-2.48		-2.48			
$4I_F$	J-K Input		-4.86		-3.96	-4.96		-4.96			
I_{FSI}	Asynchronous		-3.29		-2.48	-3.29		-3.29			
t_{pd+}					12	22			ns	Each Flip-Flop	V_{CC} = 5.0 V C_L = 15 pF
t_{pd-}					21	35			ns		
$t_{release}$					6	1			ns		
t_{set-up}				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

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